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PRE-APPEAL BRIEF REQUEST FOR REVIEW	Docket Number (Optional) 55123P265	
I hereby certify that this correspondence is being transmitted via facsimile on the date shown below to the United States Patent and Trademark Office. April 23, 2008 Signature Jessica A Clark Typed or printed name Jessica A. Clark	Application No. 10/727,230	Filed December 2, 2003
	First Named Inventor Serge Francois Drogi	
	Art Unit 2611	Examiner Vlahos, Sophia

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
NOTE: No more than five (5) pages may be provided.

I am the:

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under of 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒ Attorney or agent of record.
Registration Number 25,831

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Roger W. Blakely
Signature

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Telephone Number

April 23, 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required.

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Based on PTO/SB/33 (07-05) as modified by BSTZ (008/22/06 - WLR)
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	10/727,230	Confirmation No. 5369
Applicant	:	Serge Francois Drogi et al.	
Filed	:	04/08/2005	
TC/A.U.	:	2611	
Examiner	:	Vlahos, Sophia	
Docket No.	:	55123P265	
Customer No.	:	8791	

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REMARKS AND ARGUMENTS IN SUPPORT OF
PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

In response to the Final Office Action dated January 24, 2008, Applicants respectfully request a Pre-Appeal Panel Review of the application.

Remarks/Arguments begin on page 2 of this paper.

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REMARKS/ARGUMENTS

Claims 86-94 are pending in the present application.

A Pre-Appeal Panel Review is requested for the reason that the examiner, in her Response to Arguments presented in the first amendment, indicates that she is not considering key limitations that the undersigned believes are clearly contained in both independent claims under consideration, and which the undersigned believes clearly distinguish over the prior art. Also the claim objections in the final office action illustrate a lack of understanding of one-bit sigma delta converters, which are fundamental to the present invention, putting the entire examination in question.

The Invention

In essence, the invention is a two integrated circuit radio, one integrated circuit being an analog circuit and the other being a digital signal processor. The analog circuit provides a one-bit sigma delta modulator for output, without a data rate clock signal, to the second integrated circuit, which reconstructs the data rate clock, and recovering digital data in the received RF signal. This allows use of a standard digital signal processor, grossly reducing the development cost of a new radio by not requiring a third integrated circuit or a special digital integrated circuit.

The Examiner's Response to Arguments in First Amendment

"In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., Applicant states: 'Maligeorgos still couples a data clock between circuits, as is common in the prior art." citing column 22, lines 11-17 of U.S. 7,221,921) are not recited in the rejected claim(s)."

Independent claim 86 claims:

a first integrated circuit for receiving an RF signal and converting the RF signal to a baseband signal, and for converting the baseband signal to a serial digital signal using a one-bit sigma delta modulator for output, without a data rate clock signal, to a second integrated circuit; and

the second integrated circuit having a digital signal processor for receiving the serial digital signal output of the first integrated circuit, reconstructing the data rate clock, and recovering digital data in the received RF signal.

Independent claim 91 claims:

a first integrated circuit for receiving an RF signal and converting the RF signal to I and Q baseband signals, and for converting the baseband signals to serial digital signals using one-bit sigma delta modulators for output, without a data rate clock signal, to a second integrated circuit; and

the second integrated circuit having a digital signal processor for receiving the serial digital signal outputs of the first integrated circuit, reconstructing the data rate clock, and recovering I and Q digital data in the received RF signal by the digital signal processor;

the sigma delta modulators being controlled by a data rate clock, the data rate clock being programmable to provide various data rates in the serial digital signals for operation in various wireless communication systems.

Contrary to the examiner's position, the undersigned believes the limitation of not coupling the data rate clock from the first integrated circuit to the second integrated circuit, but instead reconstructing the data rate clock in the second integrated circuit, is clearly set out in the claims.

Claim Objections

The examiner objected to certain claims as follows:

"Claim 89 is objected to because of the following: claim 89 recites: '...is controlled by a data rate clock....' Since claim 89 depends on claim 86 that already mentions 'a data rate clock' it should be clarified whether the 'data rate clock' of claim is the same (or another data rate clock) as the data rate clock of claim 86.

Claim 90 is objected to because of the following: claim 90 recites: '...configured to convert digital data to be transmitted into a serial digital signal using a single bit delta modulator' since the single bit delta modulator is an A/D converter, the limitations is interpreted as converting digital data using a 1-bit A/D converter to serial digital data, which does not make a lot of sense.

Claims 93 and 94 recite similar limitations as the one of claim 90 above and are also objected to for the same reason."

The objection to claim 89 is not understood. Claim 96 does not mention a data rate clock, but rather the absence of a data rate clock signal output. The objection does not make sense, as how can a data rate clock be the same as a nonexistent data rate clock signal. Clocks are not signals, and particularly are not nonexistent signals.

The objection to claim 90 illustrates the examiner's lack of understanding of sigma delta modulators, which are at the heart of the present invention. It is believed that this lack of understanding puts the entire examination in question. In particular, note the statement "the limitations is interpreted as converting digital data using a 1-bit A/D converter to serial digital data, which does not make a lot of sense". In case there is any question on this point, reference is made to an article entitled "An Introduction to Delta Sigma Converters", available on the Internet. Figure 3 on page 2 of the article show a Block Diagram of a First Order Digital Delta Sigma Modulator having a digital input and a single bit digital output. The digital input is a multiple bit digital input as exemplified by the double lines at the input – also the table below Figure 3, the table headed with the statement "Likewise, in the digital modulator, the following input ranges are obtained." These input ranges correspond to 8 bit and a 16 bit inputs. The

second paragraph below Figure 3 makes specific reference to "the 1-bit DDC (digital-to-digital converter)". Again, it is believed that this lack of understanding puts the entire examination in question.

The preceding comments are also applicable to the objection to claims 93 and 94.

Rejection on Maligeorgos et al. in view of Hill

In the rejection of claims 86-88, 89, the examiner makes reference to Figure 8 of Maligeorgos, stating that his ADC (block 836) has an output, without a data rate clock, to a second integrated circuit. First, it should be noted that Maligeorgos is a three integrated circuit solution, and that Figure 8 shows a serial data output but does not show a serial clock output. However "Note that FIGS. 4 8 illustrate signal flow, rather than specific circuit implementations; for more details of the circuit implementation, for example, more details of the circuitry relating to the one-bit in-phase digital receive signal 421 and the one-bit quadrature digital receive signal 424, see FIGS. 9 14." (Col. 13, lines 31-36) Fig. 9 clearly shows serial clock signals SCLK as well as serial data SDI into and out of block 905. Clearly the examiner is wrong on this point.

The examiner does acknowledge that Maligeorgos does not teach reconstructing the data rate clock, and cites Hill for this aspect of the invention. The present inventors do not claim to be the inventors of clock recovery per se, but instead, data clock recovery in an integrated circuit rather than simply coupling the data clock from an adjacent integrated circuit (thereby avoiding a substantial source of noise). Hill recovers the clock from a subharmonic in a transmitted RF signal where no direct connection would be available. The present invention actually avoids the obvious, which would be to directly couple the data rate clock, as in Maligeorgos.

Rejection on Maligeorgos et al. in view of Hill and further in view of Khlat et al.

In the rejection of claims 89, 91-92, the examiner notes that neither Maligeorgos nor Hill teach wherein the sigma delta modulator is controlled by a data rate clock, the date rate clock being programmable to provide various data rates in thee serial digital signal for operation in various wireless communication systems, and further cites Khlat, apparently for such programmability. However the undersigned has not been able to find any such programmability in Khlat. In that regard, it appears to the undersigned that in Khlat, operation in various modes is enabled by simply replicating the sigma delta converters and using different reference frequencies for each pair of converters. (The reference to Behrens in this rejection is believed to have been intended as a reference to Hill.)

Rejection on Maligeorgos et al. in view of Hill and further in view of Sorrells et al.

Claim 90 was rejected on Maligeorgos et al. in view of Hill and further in view of Sorrells et al. Claim 90 is a dependent claim, dependent on claim 86, and further adds that "second integrated circuit is also configured to convert digital data to be transmitted into a serial digital signal using a single bit sigma delta modulator for output, without a data rate clock signal, to the first integrated circuit, and the first integrated circuit is configured to receive the serial digital signal output of the first integrated circuit, to recover the digital data to be transmitted and

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modulate the digital data for RF transmission." The examiner asserts that this limitation is disclosed by Sorrells, in that the clock is on the equivalent of the first integrated circuit and is coupled to the second integrated circuit. Consequently the clock need not be transmitted from the second integrated circuit to the first integrated circuit. However there is still a clock transmitted between the two integrated circuits, and of course claim 90 is believed allowable as dependent on an allowable independent claim.

Rejection on Maligeorgos et al. in view of Hill, Khlat et al. and Sorrells et al.

Claims 93 and 94 were rejected on Maligeorgos et al. in view of Hill, Khlat et al. and Sorrells et al, the examiner stating that these claims are rejected based on the rationale similar to the one used to reject claims 89 and 90. Of course, the same arguments presented above for claims 89 and 90 are also applicable here.

Conclusions

It is believed that the examiner does not understand one-bit sigma delta modulators, and that as a result, is reading things into the prior art to justify the rejections.

Applicant respectfully requests the Review Panel render a decision allowing the application, or at least returning the application to prosecution by an examiner who does understand such modulators.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 04/23/2008

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_____ 4/23/2008
Jessica A. Clark *Date*